Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned **"Version With Markings To Show Changes Made."**

Claim Amendments And Support For Claims

Claim 1 has been amended to recite the action of "comparing the oscillating reference against the incoming signal using a differential amplifier to detect a transition in the incoming signal relative to the known previous logical state." The differential comparison of an oscillating reference against an incoming signal using a differential amplifier to detect a transition is supported throughout the specification, and at least in FIGS. 4-1 and 4-2, and on pages 12-15. For example, in one embodiment, comparators 410A and 410B amplify the difference between the signals on their respective plus and minus inputs (e.g., see FIG. 4-1; page 12, lines 11-15). Also in one embodiment, the respective outputs of comparators 410A and 410B, via inverters 430, are indicative of whether a transition has occurred (e.g., see page 14, lines 4-13 of the specification).

Claim 2 recites, in-part, that the act of comparing of claim 1 generates a first result. Claim 2 is supported at least in FIG. 4-1 where, in one embodiment, the result of the comparison performed by comparator 410 (410A or 410B) drives output terminal 420 via inverters 430.

Claim 6 recites that the oscillating reference of claim 1 is synchronous with the input signal. Claim 6 is supported at least in FIG. 2A and on page 9, line 13 to page 10, line 2 where, in one embodiment, master 205 is described as providing single-ended signals and complementary source synchronous voltage and timing reference signals to each slave 210. Also, in that embodiment, there may be additional signals like clock or initialization for other purposes required by the protocol or synchronization of the system.

Claim 11 recites, in-part, a first controller coupled to a first comparator for coupling a first result to an output terminal based on a previous logical state. Claim 11 is supported at least in FIG. 4-1 and on page 12, line 4 to page 13, line 2 where, in one embodiment, XOR gate 425A generates a control signal for controlling switch 415A based on a comparison of a full rail SSVTR amplified signal (VT) against output signal

SN. In that embodiment, XOR gate 425A functions as a controller of switch 415A (also see arrow from XOR gate 425A to switch 415A, shown in FIG. 4-1).

Claim 20 recites, in-part, using a control signal based on the previous logical state to control whether the first result or the second result passes as an output signal. Claim 20 is supported at least in FIGS. 3B and 4-1, and on page 13, line 3 to page 14, line 13 (e.g., see page 14, lines 4-13).

Claim 23 recites, in-part, circuitry for maintaining the comparator that is coupled to the output terminal coupled to the output terminal when the new signal transitions. Claim 23 is supported at least in FIGS. 3B and 4-1, and on page 13, line 3 to page 14, line 13 (e.g., see page 14, lines 4-13).

Claims 24 and 27 recite, in-part, that the known previous logical state is a full-rail voltage. Claims 24 and 27 are supported at least in FIG. 4-1 and on page 12, lines 4-10.

It is to be understood that the above remarks regarding the present claims are provided simply to clarify the fact that the present claims are supported in the specification and that the amendments being made herein do not add new matter. That is, the present claims are not limited to the specific embodiments cited above for clarification.

Patentabilty Over US Patent No. 4,663,769 to Krinock

Applicant respectfully submits that the present claims are patentable over US Patent No. 4,663,769 to Krinock ("Krinock").

Claim 1 is patentable over Krinock at least for reciting "comparing the oscillating reference against the incoming signal using a differential amplifier to detect a transition in the incoming signal." Krinock neither discloses nor suggests the use of an oscillating reference, and its attendant benefits, for comparison with an incoming signal. At most, Krinock merely discloses the comparison of an incoming input signal with a delayed version of the same input signal (e.g., see Data, Data-90, and Data-270 for the). Note that in Krinock, the delayed version of the same input signal cannot be an oscillating reference because the input signal is a data signal, and thus cannot be oscillating (i.e., a data signal varies depending on the information being conveyed). Additionally, Krinock

neither discloses nor suggests the use of a differential amplifier, and the benefits differential signaling confers, to detect a transition. Thus, claim 1 is patentable over Krinock.

Claims 2-10, 24, and 25, which depend on claim 1, are also patentable over Krinock at least for the same reasons that claim 1 is patentable.

Claim 11 is patentable over Krinock at least for reciting comparing the oscillating reference and the incoming signal. As discussed above in connection with claim 1, Krinock neither discloses nor suggests the use of an oscillating reference, and its attendant benefits, for comparison with an incoming input signal. Thus, claim 11 is patentable over Krinock.

Claims 12-19, 26, and 27, which depend on claim 11, are also patentable over Krinock at least for the same reason that claim 11 is patentable.

Claim 20 is patentable over Krinock at least for reciting the use of an oscillating reference and a complement of the oscillating reference. As discussed above in connection with claim 1, Krinock neither discloses nor suggests the use of an oscillating reference, and its attendant benefits, for comparison with an incoming input signal. Additionally, Krinock neither discloses nor suggests comparing the incoming input signal with the oscillating reference and a complement of the oscillating reference. Thus, claim 20 is patentable over Krinock.

Claims 21 and 22, which are dependent on claim 20, are also patentable over Krinock at least for the same reasons that claim 20 is patentable.

Claim 23 is patentable over Krinock at least for reciting the use of an oscillating reference and a complement of the oscillating reference. As discussed above in connection with claim 20, Krinock neither discloses nor suggests the use of an oscillating reference for comparison with a new signal, or the comparison of the new signal with the oscillating reference and a complement of the oscillating reference. Thus, claim 23 is patentable over Krinock.

Conclusion

For at least the above reasons, claims 1-27 are in condition for allowance. If the next communication is other than a Notice Of Allowance, the Examiner is invited to telephone the undersigned attorney at (650) 843-3358.

If for any reason an insufficient fee has been paid, the Commissioner is hereby authorized to charge the insufficiency to Deposit Account No. 05-0150.

Respectfully Submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In The Claims:

Note: Claims that remain in the present application but are not being amended are reproduced herein in italics for the convenience of the Examiner. Claims that are being amended are preceded by an asterisk.

Claims 1, 4, 9, 14, 19-20, 22-23, 25, and 27 are being amended as follows:

*1. (Once Amended) A method of detecting a transition in an incoming signal from a known previous logical state, comprising:

obtaining an oscillating reference;

receiving an incoming signal; and

comparing the oscillating reference against the incoming signal using a differential amplifier to detect a transition in the incoming signal relative to the known previous logical state.

2. The method of claim 1, wherein comparing includes generating a first result; and further comprising generating a control signal based on the previous logical state for controlling whether the first result drives an output signal.

3. The method of claim 2, wherein generating the control signal includes comparing the oscillating reference and the output signal.

*4. (Once Amended) The method of claim 3, wherein the first result drives the output signal from the previous logical state toward the first result; and generating a control signal includes comparing the oscillating reference and the output signal while the output signal is still logically equal to the previous logical state.

5. The method of claim 3, wherein the first result drives the output signal from the previous logical state toward the first result; and generating a control signal includes comparing the oscillating reference and the output signal after the output signal logically equals the first result.

6. The method of claim 1, wherein the oscillating reference is synchronous with the incoming signal.

7. The method of claim 1, wherein the oscillating reference provides voltage and timing attributes.

8. The method of claim 1, wherein the oscillating reference is negated.

*9. (Once Amended) The method of claim 1, further comprising [the steps of]:

obtaining an oscillating reference complement; and comparing the complement against the incoming signal and against the previous logical state to detect a transition in the incoming signal relative to the previous logical state.

10. The method of claim 1, wherein the oscillating reference includes an oscillating source synchronous voltage, and timing reference having a slew rate and a cycle time, the slew rate being substantially equal to one-half the cycle time.

11. A system for detecting a transition in an incoming signal from a known previous logical state, comprising:

first and second input terminals for receiving, respectively, an oscillating reference and an incoming signal;

an output terminal providing an output signal logically equal to the previous logical state;

a first comparator coupled to the first and second input terminals for comparing the reference and the incoming signal to generate a first result; and

a first controller coupled to the first comparator for coupling the first result to the output terminal based on the previous logical state.

12. The system of claim 11, wherein the first controller compares the oscillating reference and the output signal.

13. The system of claim 12, wherein the first result is coupled to the output terminal to drive the output signal from the previous logical state toward the first result; and the first controller is coupled to compare the oscillating reference and the output signal while the output signal is still logically equal to the previous logical state.

*14. (Amended) The system of claim 12, wherein the first result is coupled to the output terminal to drive the output signal from the previous logical state toward the first result; and the first controller is coupled to compare the oscillating reference and the output signal [while the output signal is still logically equal to the previous logical state] after the output signal logically equals the first result.

15. The system of claim 11, wherein the oscillating reference is synchronous with the incoming signal.

16. The system of claim 11, wherein the oscillating reference provides voltage and timing attributes.

17. The system of claim 11, wherein the oscillating reference is negated.

18. The system of claim 11, wherein the oscillating reference includes an oscillating source synchronous voltage and timing reference having a slew rate and a cycle time, the slew rate being substantially equal to one-half the cycle time.

*19. (Once Amended) The system of claim 11, further comprising:

a third input terminal for receiving an oscillating reference complement;

a second comparator coupled to the second and third input terminals for comparing the complement and the incoming signal to generate a second result; and

a second controller coupled to the second comparator for coupling the second comparator to the output terminal based on the previous logical state.

*20. (Once Amended) A method of comparing an incoming signal to a previous logical state, comprising the steps of:

obtaining an oscillating reference and an oscillating reference complement, the oscillating reference complement being a complement of the oscillating reference;

receiving the incoming signal;

comparing by a first comparator the oscillating reference against the incoming signal to generate a first result;

comparing by a second comparator the oscillating reference complement against the incoming signal to generate a second result;

using a control signal based on the previous logical state to control whether the first result or the second result passes as an output signal.

21. The method of claim 20, wherein the previous logical state previously drove the output signal via the first comparator; the incoming signal is logically the same as the previous logical state; and the control signal allows the second result to pass as the output signal.

*22. (Once Amended) The method of claim 20, wherein the previous logical state previously drove the output signal via the first comparator; the incoming signal is logically opposite the previous logical state; and the control signal allows the first result to pass as the output signal.

*23. (Once Amended) A receiver comprising:

a first comparator for comparing an oscillating reference and a new signal;

a second comparator for comparing a complement of the oscillating reference and the new signal;

an output terminal coupled to one of the first and second comparators;

circuitry for maintaining the comparator that is coupled to the output terminal coupled to the output terminal when the new signal transitions; and

circuitry for coupling the other comparator to the output terminal and de-coupling the coupled comparator from the output terminal when the new signal does not transition.

24. The method of claim 1, wherein the known previous logical state is a full-rail voltage; and the oscillating reference and incoming signal are both small-swing signals.

*25. (Amended) The method of claim [20]24, wherein the small-swing signals swing approximately 0.5 volts.

26. The system of claim 11, wherein the known previous logical state is a full-rail voltage; and the oscillating reference and incoming signal are both small-swing signals.

*27. (Amended) The system of claim [20]26, wherein the small-swing signals swing approximately 0.5 volts.